Faraday RISC-V Based ASIC Solution for Edge AI and IoT SoCs

Nov., 2019

FARADAY

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Agenda

- Faraday Company Profile
- AloT ASIC Achievements
- Comprehensive IP Solutions & Low Power Design
- Platform Based Service for AIoT ASIC

Faraday Company Profile

Faraday at A Glance

Established since Y1993

- Taiwan IPO since Y1999 (TWSE: 3035)
- Commitment in ASIC & IP business

Financial status

- Capital: US\$80M
- Revenue: US\$163M (Y2018)

Top management

- Chairman: Stan Hung
- President: Steve Wang
- COO: Flash Lin



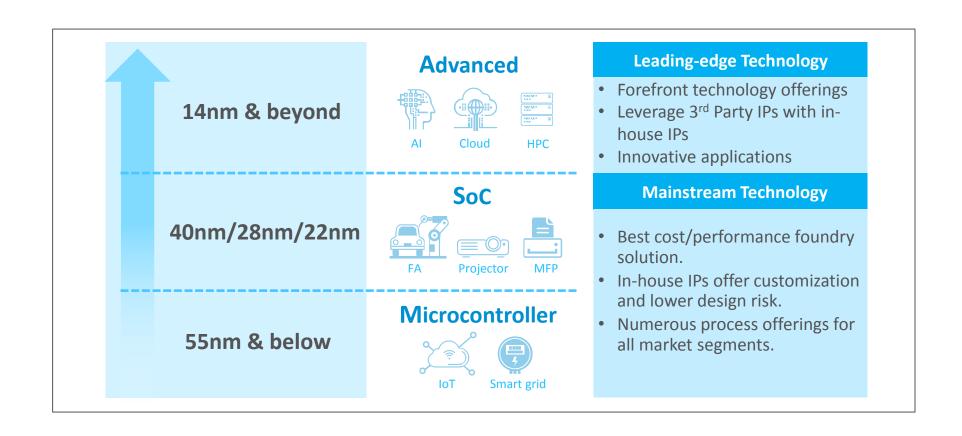


Global Deployment



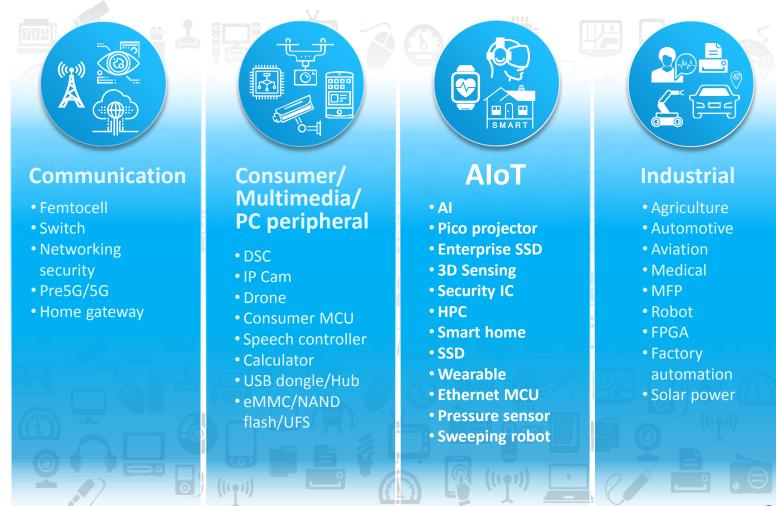


From Mainstream to Leading-edge Technology





Diversified Application Coverage

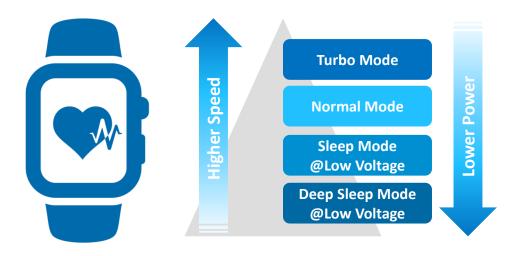


AloT ASIC Achievements



WW 1st RISC-V Based AI Wearable SoC

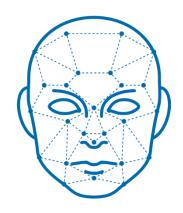
- Enabling AI Technology in Wearable Devices
 - Neural Network Hardware Accelerator
 - Support Heart ID, ECG, ECG Pro and Arrhythmia
- IP customization service
 - CPU hardness expertise
 - Analog IP customization
- Ultra low-power SoC Design
 - UMC 55ULP process
 - Support AON (Always ON)
 - Low operating voltage for long battery life
- Proven software design kit based on FreeRTOS





AloT ASIC Success Stories

- AloT SoC manufactured by 28nm, 40nm, and 55nm low power process
- PBS team helps the customer accelerate time-to-market
- Applications covering 3D face recognition, drone vision, voice recognition, and language translation, etc.











Comprehensive IP Solutions & Low Power Design



Comprehensive IP Portfolio

SoC Peripherals

- Bus switch
- Bus bridge/controller
- DMA controller
- Interrupt controller
- Memory controller
- RTC, UART, GPIO, watch dog timer

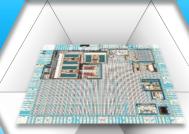
Analog & IO

- PLL, SSCG PLL, DLL, RC OSC
- LDO, PWM, POR, VDT
- ADC, DAC, Audio Codec
- GPIO, High-V tolerant IO, Multi-V IO, Customized IO

Processor Cores

- ARM cortex (A-, R-, M-)
- Faraday: FA616TE, FA626TI
- Synopsys: DSP, CNN

Andes RISC-V



Library

- Standard cell libraries
- Multi-track, multi-Vt, multi channel length, multi-voltage
- Feature libraries
- _ miniLib™ PowerSlash™
- _ UHS-Lib™ M1+ ™
- _ UrLib+® Add-on

High-speed IO

- DDR/LPDDR, GDDR, HBM, ONFi
- Programmable Serdes, USB, PCI Express, SATA, Ethernet 10/100/1000
- LVDS, subLVDS, mLVDS, MIPI, V-by-one

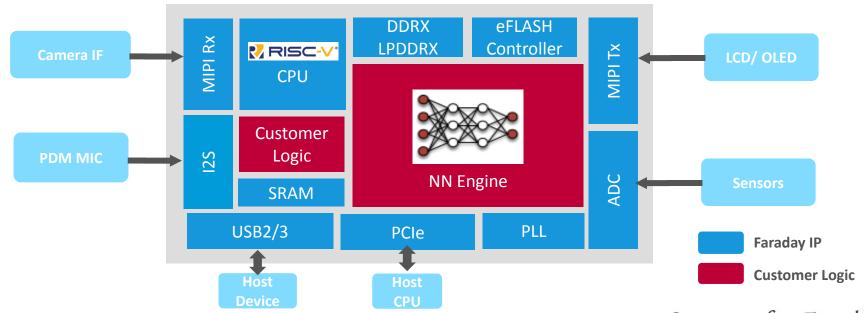
Memory

- SRAM compiler
- Logic & eHV MemMaker™
- SRAM, ROM, register file
- efuse, OTP, MTP
- eFlash, eMRAM



Total Solution Block Diagram of AI Edge Computing

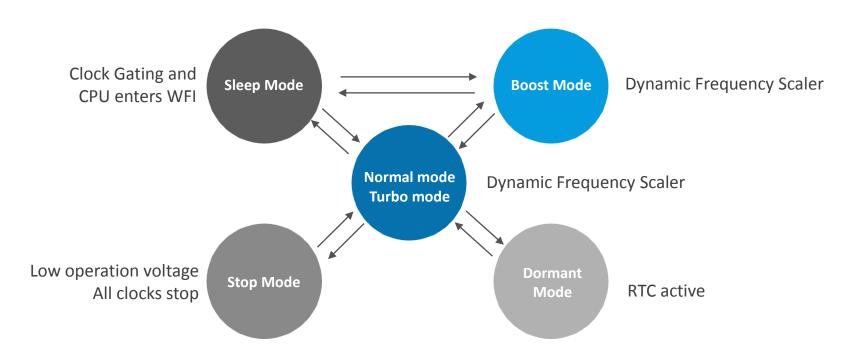
- Broad Applications: Surveillance, Smart wristband, Smart speaker, etc.
- CPU Harden for performance optimization
- In-house IP Customization: SRAM, eFlash, DDR/LPDDR, MIPI, USB, PCIe, PLL, ADC, etc.
- Wide Process Adoption: 55nm/40nm/28nm/22nm





Low Power SoC Design and DVFS

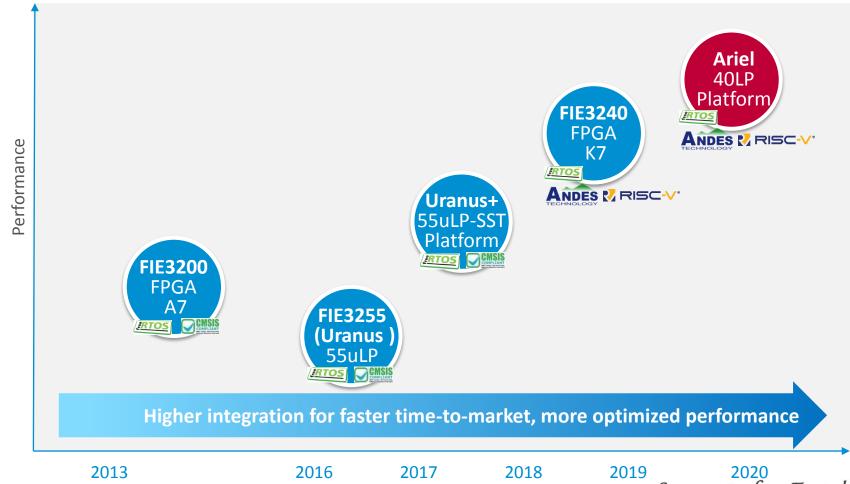
- **Power Domain Partition**
- **DVFS (dynamic voltage and frequency scaling)**
- Micro program sequence engine for power saving



Platform Based Service for AIoT ASIC



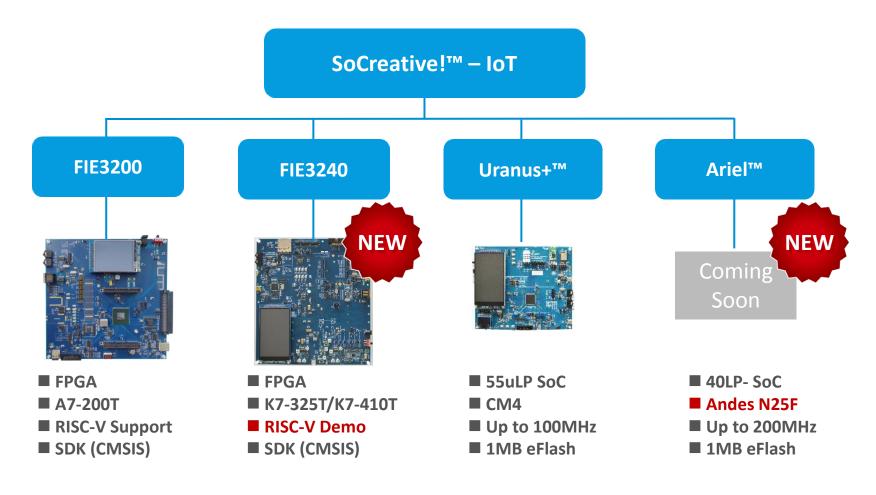
SoCreative!™ IoT SoC Platform Development Roadmap



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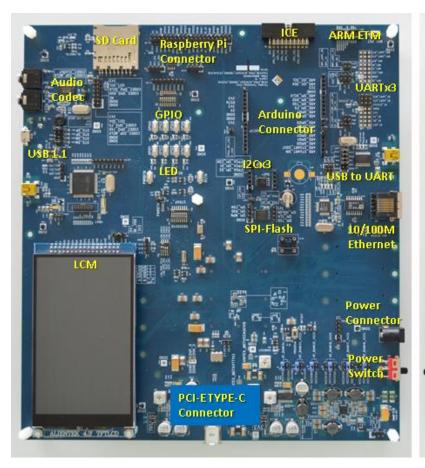


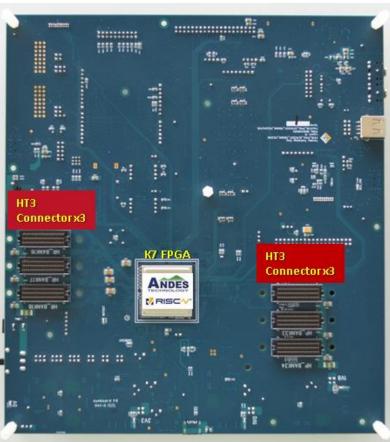
SoCreative!™ IoT SoC Platforms





FIE3240 Demo



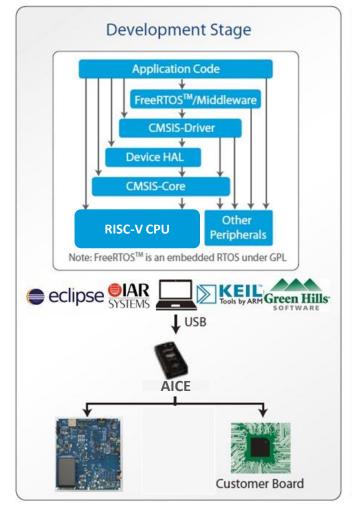


Features:

- Xlilinx K7 FPGA
- Supports PCle-to-PCle interconnect
 - High speed type-C connector
 - FPGA2FPGA, FPGA2ASIC communication
- HT3 daughter boards
 - Enable USB3, MIPI, GPHY,
 DDR functions
- Multiple Voltage IO
 - 1.8V/2.5V/3.3V



FIE3240 Development Environment







Ariel™ Platform

- UMC 40nm process with 1Mbits eFlash SoC
- Andes N25F RISC-V CPU
- Ultra low-power design with power partitions and DVFS
- IoT gateway and node demonstrations





Summary: Why Faraday?

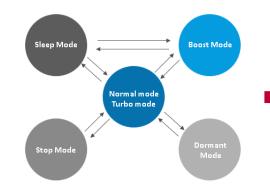
Comprehensive IP Portfolio



SoCreative!™ IoT SoC Platform



Low Power Design Methodology



Your Idea







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